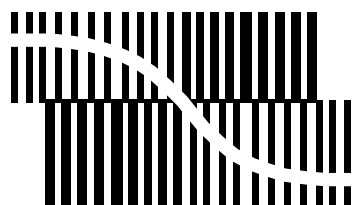


DATA SHEET



BITSTREAM CONVERSION

UDA1351TS 96 kHz IEC 958 audio DAC

Product specification
Supersedes data of 2000 Mar 28
File under Integrated Circuits, IC01

2001 Feb 05

96 kHz IEC 958 audio DAC**UDA1351TS**

| | | |
|---|------|--|
| CONTENTS | 9 | LIMITING VALUES |
| 1 FEATURES | 10 | THERMAL CHARACTERISTICS |
| 1.1 General | 11 | CHARACTERISTICS |
| 1.2 Control | 12 | TIMING CHARACTERISTICS |
| 1.3 IEC 958 input | 13 | APPLICATION INFORMATION |
| 1.4 Digital sound processing and DAC | 14 | PACKAGE OUTLINE |
| 2 APPLICATIONS | 15 | SOLDERING |
| 3 GENERAL DESCRIPTION | 15.1 | Introduction to soldering surface mount packages |
| 4 QUICK REFERENCE DATA | 15.2 | Reflow soldering |
| 5 ORDERING INFORMATION | 15.3 | Wave soldering |
| 6 BLOCK DIAGRAM | 15.4 | Manual soldering |
| 7 PINNING | 15.5 | Suitability of surface mount IC packages for wave and reflow soldering methods |
| 8 FUNCTIONAL DESCRIPTION | 16 | DEFINITIONS |
| 8.1 Clock regeneration and lock detection | 17 | LIFE SUPPORT APPLICATIONS |
| 8.2 Mute | | |
| 8.3 Auto mute | | |
| 8.4 Data path | | |
| 8.4.1 IEC 958 input | | |
| 8.4.2 Audio feature processor | | |
| 8.4.3 Interpolator | | |
| 8.4.4 Noise shaper | | |
| 8.4.5 The Filter Stream DAC (FSDAC) | | |
| 8.5 Control | | |
| 8.5.1 Static pin control mode | | |
| 8.5.2 L3 control mode | | |
| 8.6 L3 interface | | |
| 8.6.1 General | | |
| 8.6.2 Device addressing | | |
| 8.6.3 Register addressing | | |
| 8.6.4 Data write mode | | |
| 8.6.5 Data read mode | | |
| 8.6.6 initialization string | | |
| 8.6.7 Overview of L3 interface registers | | |
| 8.6.8 Writable registers | | |
| 8.6.9 Readable registers | | |

96 kHz IEC 958 audio DAC

UDA1351TS

1 FEATURES**1.1 General**

- 2.7 to 3.6 V power supply
- Integrated digital filter and Digital-to-Analog Converter (DAC)
- Master-mode data output and input interface for off-chip sound processing
- $256f_s$ system clock output
- 20-bit data path in interpolator
- High performance
- No analog post filtering required for DAC
- Support sampling frequencies from 28 kHz up to 100 kHz
- The UDA1351TS is fully pin and function compatible with the UDA1350ATS.

1.2 Control

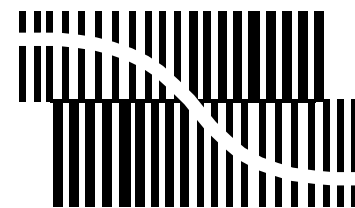
Controlled either by means of static pins or via the L3 microcontroller interface.

1.3 IEC 958 input

- On-chip amplifier for converting IEC 958 input to CMOS levels
- Lock indication signal available on pin LOCK
- Lock indication signal combined on-chip with the Pulse Code Modulation (PCM) status bit; when non-PCM is detected, pin LOCK indicates out-of-lock
- Key channel-status bits available via L3 interface (lock, pre-emphasis, audio sample frequency, two channel PCM indication and clock accuracy).

1.4 Digital sound processing and DAC

- Automatic de-emphasis when using IEC 958 input with 32.0, 44.1 and 48.0 kHz audio sample frequencies
- Soft mute by means of a cosine roll-off circuit selectable via pin MUTE or the L3 interface
- dB linear volume control with 1 dB steps from 0 dB to -60 dB and $-\infty$ dB
- Bass boost and treble control in L3 control mode
- Interpolating filter (f_s to $128f_s$) by means of a cascade of a recursive filter and a FIR filter
- Third order noise shaper operating at $128f_s$ generates the bitstream for the DAC
- Filter Stream DAC (FSDAC).



BITSTREAM CONVERSION

2 APPLICATIONS

Digital audio systems.

3 GENERAL DESCRIPTION

Available in two versions:

- UDA1351TS:
 - only IEC 958 input to DAC in SSOP28 package.
- UDA1351H:
 - full featured version in QFP44 package.

The UDA1351TS is a single chip IEC 958 audio decoder with an integrated stereo DAC employing bitstream conversion techniques.

A lock indication signal is available on pin LOCK, indicating that the IEC 958 decoder is locked. This pin is also used to indicate whether PCM data is applied to the input or not. When non-PCM data is detected, the device indicates out-of-lock.

By default, the DAC output and the data output interface are muted when the decoder is out-of-lock. However, this setting can be overruled in the L3 control mode.

96 kHz IEC 958 audio DAC

UDA1351TS

4 QUICK REFERENCE DATA

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|------------------------------------|--|---|------|------|------|------|
| Supplies | | | | | | |
| V _{DDD} | digital supply voltage | | 2.7 | 3.0 | 3.6 | V |
| V _{DDA} | analog supply voltage | | 2.7 | 3.0 | 3.6 | V |
| I _{DDA(DAC)} | analog supply current of DAC | power-on | – | 8.0 | – | mA |
| | | Power-down | – | 750 | – | μA |
| I _{DDA(PLL)} | analog supply current of PLL | at 48 kHz | – | 0.7 | – | mA |
| | | at 96 kHz | – | 1.0 | – | mA |
| I _{DDD(C)} | digital supply current of core | at 48 kHz | – | 16.0 | – | mA |
| | | at 96 kHz | – | 24.5 | – | mA |
| I _{DDD} | digital supply current | at 48 kHz | – | 2.0 | – | mA |
| | | at 96 kHz | – | 3.0 | – | mA |
| P | power consumption at 48 kHz | DAC in playback mode | – | 80 | – | mW |
| | | DAC in Power-down mode | – | 58 | – | mW |
| | power consumption at 96 kHz | DAC in playback mode | – | 109 | – | mW |
| | | DAC in Power-down mode | – | 87 | – | mW |
| General | | | | | | |
| t _{rst} | reset active time | | – | 250 | – | μs |
| T _{amb} | ambient temperature | | –40 | – | +85 | °C |
| Digital-to-analog converter | | | | | | |
| V _{o(rms)} | output voltage (RMS value) | note 1 | – | 900 | – | mV |
| (THD + N)/S | total harmonic distortion-plus-noise to signal ratio | f _i = 1.0 kHz tone at 48 kHz | – | –90 | –85 | dB |
| | | at 0 dB | – | –60 | –55 | dB |
| | | at –40 dB; A-weighted | – | –85 | –80 | dB |
| | | at –40 dB; A-weighted | – | –57 | –52 | dB |
| S/N | signal-to-noise ratio at 48 kHz | f _i = 1.0 kHz tone; code = 0; A-weighted | 95 | 100 | – | dB |
| | signal-to-noise ratio at 96 kHz | f _i = 1.0 kHz tone; code = 0; A-weighted | 95 | 100 | – | dB |
| α _{CS} | channel separation | f _i = 1.0 kHz tone | – | 96 | – | dB |
| ΔV _o | unbalance of output voltages | f _i = 1.0 kHz tone | – | 0.1 | 0.4 | dB |

Note

1. The output voltage of the DAC is proportional to the DAC power supply voltage.

5 ORDERING INFORMATION

| TYPE NUMBER | PACKAGE | | |
|-------------|---------|---|----------|
| | NAME | DESCRIPTION | VERSION |
| UDA1351TS | SSOP28 | plastic shrink small outline package; 28 leads; body width 5.3 mm | SOT341-1 |

96 kHz IEC 958 audio DAC

UDA1351TS

6 BLOCK DIAGRAM

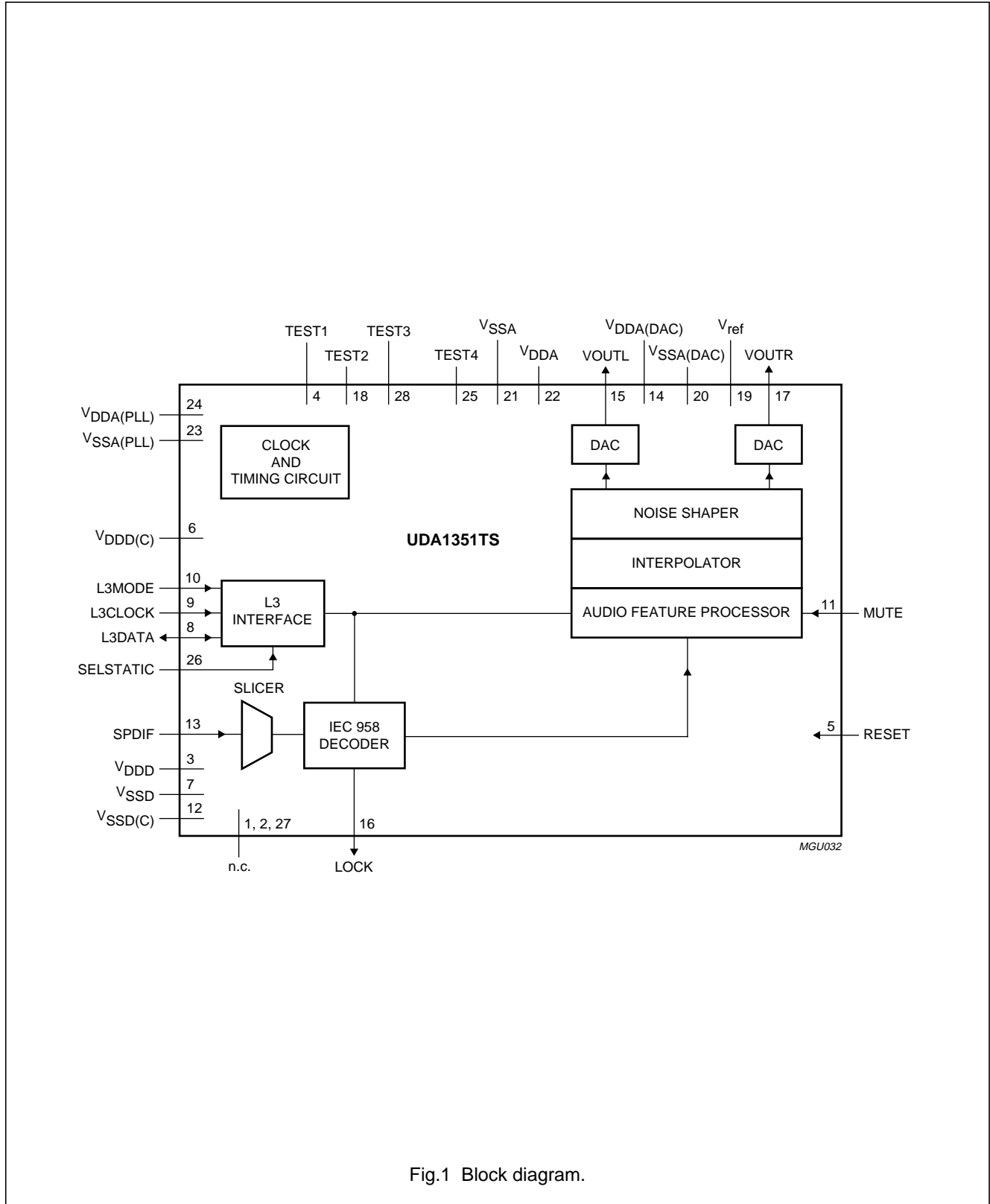


Fig.1 Block diagram.

96 kHz IEC 958 audio DAC

UDA1351TS

7 PINNING

| SYMBOL | PIN | TYPE ⁽¹⁾ | DESCRIPTION |
|-----------------------|-----|---------------------|---|
| n.c. | 1 | – | not connected |
| n.c. | 2 | – | not connected |
| V _{DDD} | 3 | DS | digital supply voltage |
| TEST1 | 4 | DID | test pin 1; must be connected to digital ground (V _{SSD}) |
| RESET | 5 | DISD | reset input |
| V _{DDD(C)} | 6 | DS | digital supply voltage for core |
| V _{SSD} | 7 | DGND | digital ground |
| L3DATA | 8 | DIOS | L3 interface data input and output |
| L3CLOCK | 9 | DIS | L3 interface clock input |
| L3MODE | 10 | DIS | L3 interface mode input |
| MUTE | 11 | DID | mute control input |
| V _{SSD(C)} | 12 | DGND | digital ground |
| SPDIF | 13 | AI | IEC 958 channel input |
| V _{DDA(DAC)} | 14 | AS | analog supply voltage for DAC |
| VOU _{TL} | 15 | AO | analog DAC left channel output |
| LOCK | 16 | DO | SPDIF and PLL lock indicator output |
| VOU _{TR} | 17 | AO | analog DAC right channel output |
| TEST2 | 18 | DID | test pin 2; must be connected to digital ground (V _{SSD}) |
| V _{ref} | 19 | A | DAC reference voltage |
| V _{SSA(DAC)} | 20 | AGND | analog ground for DAC |
| V _{SSA} | 21 | AGND | analog ground |
| V _{DDA} | 22 | AS | analog supply voltage |
| V _{SSA(PLL)} | 23 | AGND | analog ground for PLL |
| V _{DDA(PLL)} | 24 | AS | analog supply voltage for PLL |
| TEST4 | 25 | DIU | test pin 4; must be connected to the digital supply voltage (V _{DDD}) |
| SELSTATIC | 26 | DIU | static pin control selection input |
| n.c. | 27 | – | not connected |
| TEST3 | 28 | DISD | test pin 3; must be connected to digital ground (V _{SSD}) |

Note

1. See Table 1.

96 kHz IEC 958 audio DAC

UDA1351TS

Table 1 Pin type references

| PIN TYPE | DESCRIPTION |
|----------|--|
| DS | digital supply |
| DGND | digital ground |
| AS | analog supply |
| AGND | analog ground |
| DI | digital input |
| DIS | digital Schmitt-triggered input |
| DID | digital input with internal pull-down resistor |
| DISD | digital Schmitt-triggered input with internal pull-down resistor |
| DIU | digital input with internal pull-up resistor |
| DO | digital output |
| DIO | digital input and output |
| DIOS | digital Schmitt-triggered input and output |
| A | analog reference voltage |
| AI | analog input |
| AO | analog output |

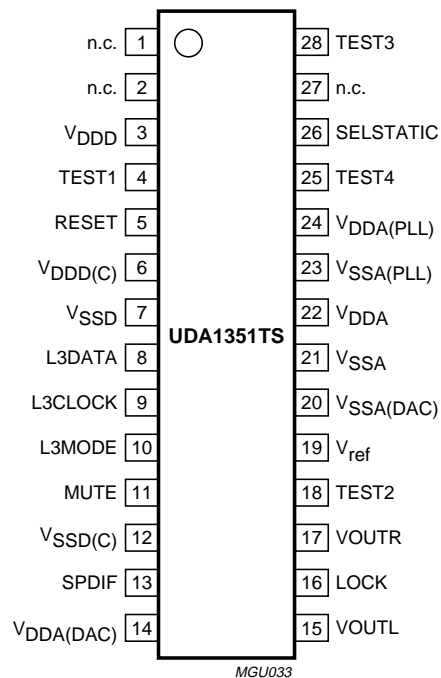


Fig.2 Pin configuration.

96 kHz IEC 958 audio DAC

UDA1351TS

8 FUNCTIONAL DESCRIPTION

The UDA1351TS is a low cost audio IEC 958 decoder with an on-board DAC. The minimum audio input sampling frequency conforming to the IEC958 standard is 28.0 kHz and the maximum audio sampling frequency is 100.0 kHz.

8.1 Clock regeneration and lock detection

The UDA1351TS contains an on-board PLL for regenerating a system clock from the IEC 958 input bitstream.

Note: If there is no input signal, the PLL generates a minimum frequency and the output spectrum shifts accordingly. Since the analog output does not have an analog mute, this means noise that is out of band under normal conditions can move into the audio band.

When the on-board clock locks to the incoming frequency, the lock indicator bit is set and can be read via the L3 interface. Internally, the PLL lock indication is combined with the PCM status bit of the input data stream. When both the IEC 958 decoder and the on-board clock have locked to the incoming signal and the input data stream is PCM data, pin LOCK will be asserted. However, when the IC is locked but the PCM status bit reports non-PCM data, pin LOCK is returned to LOW level.

The lock indication output can be used, for example, for muting purposes. The lock signal can be used to drive an external analog muting circuit to prevent out of band noise from becoming audible when the PLL runs at its minimum frequency (e.g. when there is no SPDIF input signal).

An example of the mute circuit is illustrated in Fig.3 where V_{DD} is the positive power supply and V_{SS} is the negative power supply.

8.2 Mute

The UDA1351TS is equipped with a cosine roll-off mute in the DSP data path of the DAC part. Muting the DAC, by pin MUTE (in static mode) or via bit MT (in L3 mode), will result in a soft mute, as shown in Fig.4. The cosine roll-off soft mute takes 32×32 samples = 24 ms at 44.1 kHz sampling frequency.

When operating in the L3 control mode, the device will mute on start-up. In L3 mode, it is necessary to explicitly switch off the mute for audio output by means of the MT bit in the L3 register.

In the L3 mode, pin MUTE does not have any function (the same holds for several other pins) and can either be left open-circuit (since it has an internal pull-down resistor) or be connected to ground.

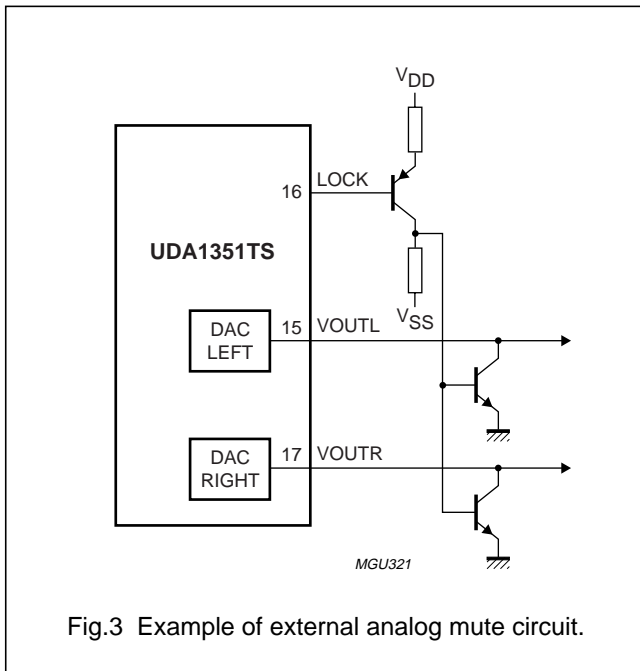


Fig.3 Example of external analog mute circuit.

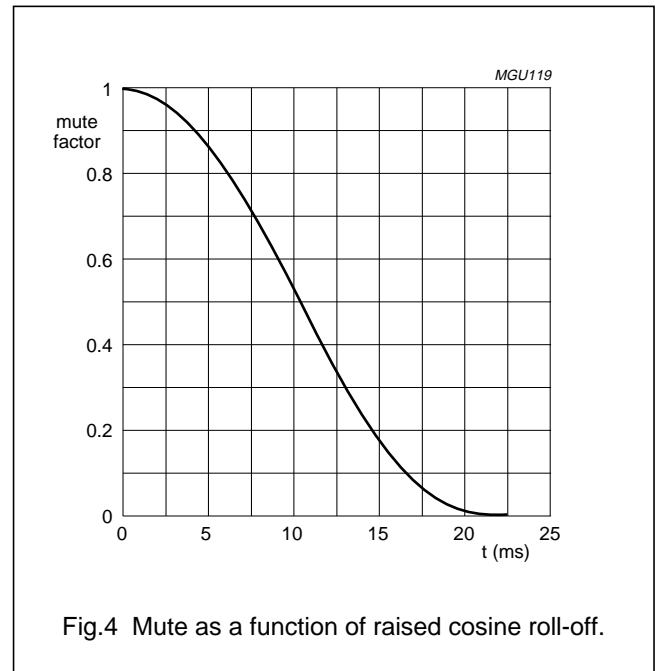


Fig.4 Mute as a function of raised cosine roll-off.

96 kHz IEC 958 audio DAC

UDA1351TS

8.3 Auto mute

By default, the DAC outputs will be muted until the IC is locked, regardless of the level on pin MUTE (in static mode) or the state of bit MT of the sound feature register (in L3 mode). In this way, only valid data will be passed to the outputs. This mute is done in the SPDIF interface and is a hard mute, not a cosine roll-off mute.

If needed, this muting can be bypassed by setting bit AutoMT to logic 0 via the L3 interface. As a result, the IC will no longer mute during out-of-lock situations.

8.4 Data path

The UDA1351TS data path consists of the IEC 958 decoder, the audio feature processor, digital interpolator and noise shaper and the DACs.

8.4.1 IEC 958 INPUT

The UDA1351TS IEC 958 decoder features an on-chip amplifier with hysteresis, which amplifies the IEC 958 input signal to CMOS level (see Fig.5).

All 24 bits of data for left and right are extracted from the input bitstream as well as several of the IEC 958 key channel-status bits.

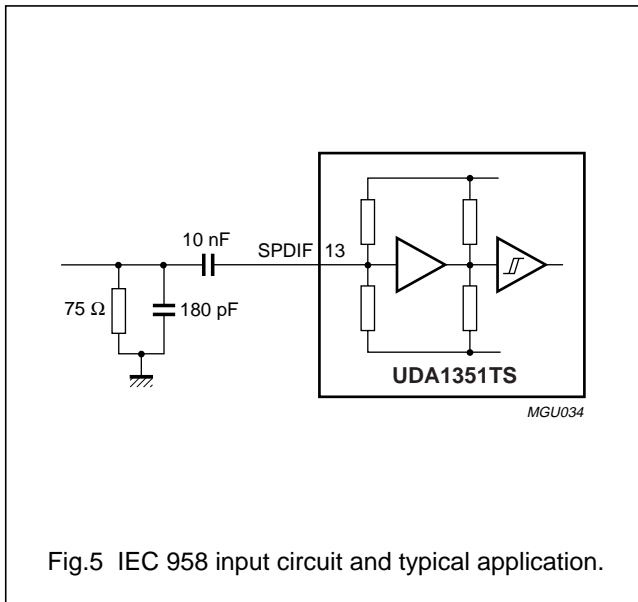


Fig.5 IEC 958 input circuit and typical application.

The extracted key parameters are:

- Pre-emphasis
- Audio sample frequency
- Two-channel PCM indicator
- Clock accuracy.

Both the lock indicator and the key channel status bits are accessible via the L3 interface.

The UDA1351TS supports the following sample frequencies and data bit rates:

- $f_s = 32.0$ kHz, resulting in a data rate of 2.048 Mbits/s
- $f_s = 44.1$ kHz, resulting in a data rate of 2.8224 Mbits/s
- $f_s = 48.0$ kHz, resulting in a data rate of 3.072 Mbits/s
- $f_s = 64.0$ kHz, resulting in a data rate of 4.096 Mbits/s
- $f_s = 88.2$ kHz, resulting in a data rate of 5.6448 Mbits/s
- $f_s = 96.0$ kHz, resulting in a data rate of 6.144 Mbits/s.

The UDA1351TS supports timing levels I, II and III, as specified by the IEC 958 standard.

8.4.2 AUDIO FEATURE PROCESSOR

The audio feature processor automatically provides de-emphasis for the IEC 958 data stream in the static pin control mode and default mute at start-up in the L3 control mode.

When used in the L3 control mode, it provides the following additional features:

- Volume control, using 6 bits
- Bass boost control, using 4 bits
- Treble control, using 2 bits
- Mode selection of the sound processing bass boost and treble filters: flat, minimum and maximum
- Soft mute control with raised cosine roll-off
- De-emphasis selection of the incoming data stream for $f_s = 32.0, 44.1$ and 48.0 kHz.

8.4.3 INTERPOLATOR

The UDA1351TS includes an on-board interpolating filter which converts the incoming data stream from $1f_s$ to $128f_s$ by cascading a recursive filter and a FIR filter.

96 kHz IEC 958 audio DAC

UDA1351TS

Table 2 Interpolator characteristics

| PARAMETER | CONDITIONS | VALUE (dB) |
|------------------|----------------|------------|
| Pass-band ripple | 0 to $0.45f_s$ | ± 0.03 |
| Stop band | $>0.65f_s$ | -50 |
| Dynamic range | 0 to $0.45f_s$ | 115 |
| DC gain | - | -3.5 |

8.4.4 NOISE SHAPER

The third-order noise shaper operates at $128f_s$. It shifts in-band quantization noise to frequencies well above the audio band. This noise shaping technique enables high signal-to-noise ratios to be achieved. The noise shaper output is converted to an analog signal using a filter stream DAC.

8.4.5 THE FILTER STREAM DAC (FSDAC)

The FSDAC is a semi-digital reconstruction filter that converts the 1-bit data stream of the noise shaper to an analog output voltage. The filter coefficients are implemented as current sources and are summed at virtual ground of the output operational amplifier. In this way, very high signal-to-noise performance and low clock jitter sensitivity is achieved.

A post-filter is not needed due to the inherent filter function of the DAC. On-board amplifiers convert the FSDAC output current to an output voltage signal capable of driving a line output.

The output voltage of the FSDAC is scaled proportionally with the power supply voltage.

8.5 Control

The UDA1351TS can be controlled by means of static pins or via the L3 interface. For optimum use of the features of the UDA1351TS, the L3 control mode is recommended since only basic functions are available in the static pin control mode.

It should be noted that the static pin control mode and L3 control mode are mutually exclusive. In the static pin control mode, pins L3MODE and L3DATA are used to select the format for the data output and input interface.

8.5.1 STATIC PIN CONTROL MODE

The default values for all non-pin controlled settings are identical to the default values at start-up in the L3 control mode.

Table 3 Pin description of static pin control mode

| PIN | NAME | VALUE | FUNCTION |
|---------------------------|-----------|-------|---|
| Mode selection pin | | | |
| 26 | SELSTATIC | 1 | select static pin control mode; must be connected to V_{DD} |
| Input pins | | | |
| 5 | RESET | 0 | normal operation |
| | | 1 | reset |
| 8 | L3DATA | 0 | must be connected to V_{SSD} |
| 9 | L3CLOCK | 0 | must be connected to V_{SSD} |
| 10 | L3MODE | 0 | must be connected to V_{SSD} |
| 11 | MUTE | 0 | normal operation |
| | | 1 | mute active |
| Status pin | | | |
| 16 | LOCK | 0 | clock regeneration and IEC 958 decoder out-of-lock or non-PCM data detected |
| | | 1 | clock regeneration and IEC 958 decoder locked and PCM data detected |

96 kHz IEC 958 audio DAC

UDA1351TS

| PIN | NAME | VALUE | FUNCTION |
|------------------|-------|-------|---|
| Test pins | | | |
| 4 | TEST1 | 0 | must be connected to digital ground (V_{SSD}) |
| 18 | TEST2 | 0 | must be connected to digital ground (V_{SSD}) |
| 25 | TEST4 | 1 | must be connected to digital supply voltage (V_{DDD}) |
| 28 | TEST3 | 0 | must be connected to digital ground (V_{SSD}) |

8.5.2 L3 CONTROL MODE

The L3 control mode allows maximum flexibility in controlling the UDA1351TS.

It should be noted that, in the L3 control mode, several base-line functions are still controlled by pins on the device and that, on start-up in the L3 control mode, the output is explicitly muted by bit MT via the L3 interface.

Table 4 Pin description in the L3 control mode

| PIN | NAME | VALUE | FUNCTION |
|---------------------------|-----------|-------|---|
| Mode selection pin | | | |
| 26 | SELSTATIC | 0 | select L3 control mode; must be connected to V_{SSD} |
| Input pins | | | |
| 5 | RESET | 0 | normal operation |
| | | 1 | reset |
| 8 | L3DATA | – | must be connected to the L3-bus |
| 9 | L3CLOCK | – | must be connected to the L3-bus |
| 10 | L3MODE | – | must be connected to the L3-bus |
| Status pin | | | |
| 16 | LOCK | 0 | clock regeneration and IEC 958 decoder out-of-lock or non-PCM data detected |
| | | 1 | clock regeneration and IEC 958 decoder locked and PCM data detected |
| Test pins | | | |
| 4 | TEST1 | 0 | must be connected to ground (V_{SSD}) |
| 18 | TEST2 | 0 | must be connected to ground (V_{SSD}) |
| 25 | TEST4 | 1 | must be connected to digital supply voltage (V_{DDD}) |
| 28 | TEST3 | 0 | must be connected to ground (V_{SSD}) |

96 kHz IEC 958 audio DAC

UDA1351TS

8.6 L3 interface**8.6.1 GENERAL**

The UDA1351TS has an L3 microcontroller interface and all the digital sound processing features and various system settings can be controlled by a microcontroller.

The controllable settings are:

- Restoring L3 defaults
- Power-on
- Selection of filter mode and settings of treble and bass boost
- Volume settings
- Selection of soft mute via cosine roll-off and bypass of auto mute
- Selection of de-emphasis (only effective in L3 control mode).

The readable settings are:

- Mute status of interpolator
- PLL locked
- SPDIF input signal locked
- Audio Sample Frequency (ASF)
- Valid PCM data detected
- Pre-emphasis of the IEC 958 input signal
- ACcuracy of the Clock (ACC).

The exchange of data and control information between the microcontroller and the UDA1351TS is LSB first and is accomplished through a serial hardware L3 interface comprising the following pins:

- L3DATA: data line
- L3MODE: mode line
- L3CLK: clock line.

The exchange of bytes via the L3 interface is LSB first.

The L3 format has two modes of operation:

- Address mode
- Data transfer mode.

The address mode is used to select a device for a subsequent data transfer. The address mode is characterized by L3MODE being LOW and a burst of 8 pulses on L3CLOCK, accompanied by eight bits (see Fig.6). The data transfer mode is characterized by L3MODE being HIGH and is used to transfer one or more bytes representing a register address, instruction or data.

Basically, two types of data transfers can be defined:

- Write action: data transfer **to** the device
- Read action: data transfer **from** the device.

Remark: when the device is powered up, at least one L3CLOCK pulse must be given to the L3 interface to wake up the interface before starting sending to the device, see Fig.6. This is only needed once after the device is powered up.

8.6.2 DEVICE ADDRESSING

The device address consists of one byte with:

- Data Operating Mode (DOM) bits 0 and 1 representing the type of data transfer (see Table 5)
- Address bits 2 to 7 representing a 6-bit device address.

Table 5 Selection of data transfer

| DOM | | TRANSFER |
|-------|-------|----------------------------|
| BIT 0 | BIT 1 | |
| 0 | 0 | not used |
| 1 | 0 | not used |
| 0 | 1 | write data or prepare read |
| 1 | 1 | read data |

8.6.3 REGISTER ADDRESSING

After sending the device address (including DOM bits), indicating whether the information is to be read or written, one data byte is sent using bit 0 to indicate whether the information will be read or written and bits 1 to 7 for the destination register address.

Basically, there are three methods for register addressing:

1. Addressing for write data: bit 0 is logic 0 indicating a write action to the destination register, followed by bits 1 to 7 indicating the register address (see Fig.6)
2. Addressing for prepare read: bit 0 is logic 1, indicating that data will be read from the register (see Fig.7)
3. Addressing for data read action. Here, the device returns a register address prior to sending data from that register. When bit 0 is logic 0, the register address is valid; when bit 0 is logic 1, the register address is invalid.

96 KHz IEC 958 audio DAC

UDA1351TS

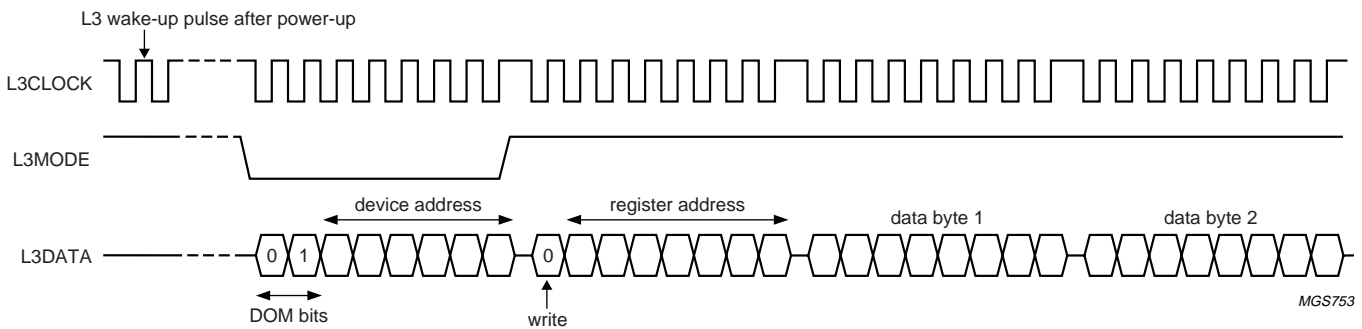


Fig.6 Data write mode (for L3 version 2).

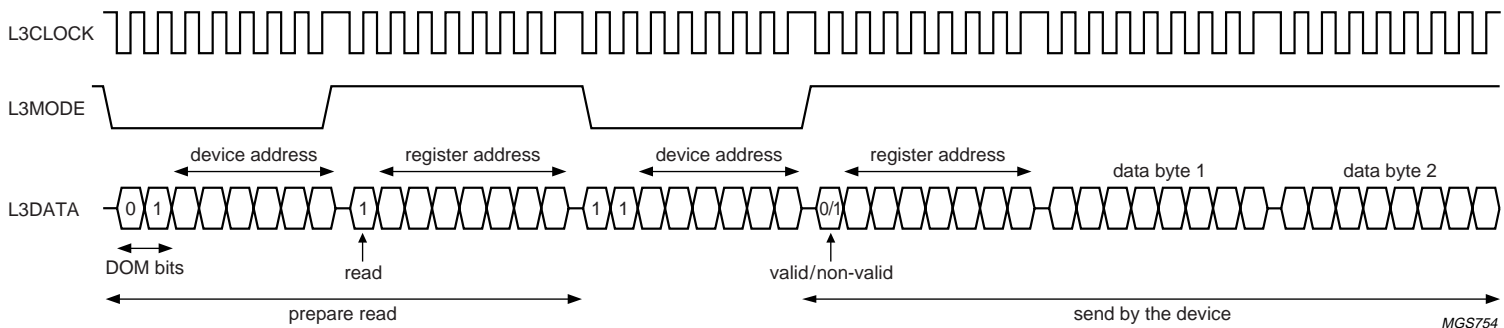


Fig.7 Data read mode.

96 kHz IEC 958 audio DAC

UDA1351TS

8.6.4 DATA WRITE MODE

The data write mode is explained in the signal diagram of Fig.6. For writing data to a device, four bytes must be sent (see Table 6):

1. One byte starting with '01' for signalling the write action to the device, followed by the device address ('011000' for the UDA1351TS)
2. One byte starting with a '0' for signalling the write action, followed by seven bits indicating the destination address in binary format with A6 being the MSB and A0 being the LSB
3. Two data bytes with D15 being the MSB and D0 being the LSB.

It should be noted that each time a new destination register address needs to be written, the device address must be sent again.

8.6.5 DATA READ MODE

To read data from the device, a prepare read must first be done and then data read. The data read mode is explained in the signal diagram of Fig.7.

For reading data from a device, the following six bytes are involved (see Table 7):

1. One byte with the device address, including '01' for signalling the write action to the device
2. One byte is sent with the register address from which data needs to be read. This byte starts with a '1', which indicates that there will be a read action from the register, followed again by seven bits for the destination address in binary format, with A6 being the MSB and A0 being the LSB
3. One byte with the device address, including '11' is sent to the device. The '11' indicates that the device must write data to the microcontroller
4. One byte, sent by the device to the bus, with the (requested) register address and a flag bit indicating whether the requested register was valid (bit is logic 0) or invalid (bit is logic 1)
5. Two bytes, sent by the device to the bus, with the data information in binary format, with D15 being the MSB and D0 being the LSB.

Table 6 L3 write data

| BYTE | L3 MODE | ACTION | FIRST IN TIME | | | | LATEST IN TIME | | | |
|------|---------------|------------------|---------------|-------|-------|-------|----------------|-------|-------|-------|
| | | | BIT 0 | BIT 1 | BIT 2 | BIT 3 | BIT 4 | BIT 5 | BIT 6 | BIT 7 |
| 1 | address | device address | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 |
| 2 | data transfer | register address | 0 | A6 | A5 | A4 | A3 | A2 | A1 | A0 |
| 3 | data transfer | data byte 1 | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 |
| 4 | data transfer | data byte 2 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |

Table 7 L3 read data

| BYTE | L3 MODE | ACTION | FIRST IN TIME | | | | LATEST IN TIME | | | |
|------|---------------|------------------|---------------|-------|-------|-------|----------------|-------|-------|-------|
| | | | BIT 0 | BIT 1 | BIT 2 | BIT 3 | BIT 4 | BIT 5 | BIT 6 | BIT 7 |
| 1 | address | device address | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 |
| 2 | data transfer | register address | 1 | A6 | A5 | A4 | A3 | A2 | A1 | A0 |
| 3 | address | device address | 1 | 1 | 0 | 1 | 1 | 0 | 0 | 0 |
| 4 | data transfer | register address | 0 or 1 | A6 | A5 | A4 | A3 | A2 | A1 | A0 |
| 5 | data transfer | data byte 1 | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 |
| 6 | data transfer | data byte 2 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |

96 kHz IEC 958 audio DAC

UDA1351TS

8.6.6 INITIALIZATION STRING

For proper and reliable operation, the UDA1351TS must be initialized in the L3 control mode. This is required to have the PLL start up after powering up of the device under all conditions. The initialization string is given in Table 8.

Table 8 L3 initialization string and set defaults after power-up.

| BYTE | L3 MODE | ACTION | | FIRST IN TIME | | | | | LATEST IN TIME | | |
|------|---------------|--------------|------------------|---------------|-------|-------|-------|-------|----------------|-------|-------|
| | | | | BIT 0 | BIT 1 | BIT 2 | BIT 3 | BIT 4 | BIT 5 | BIT 6 | BIT 7 |
| 1 | address | init string | device address | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 |
| 2 | data transfer | | register address | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| 3 | data transfer | | data byte 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 4 | data transfer | | data byte 2 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |
| 5 | address | set defaults | device address | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 |
| 6 | data transfer | | register address | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| 7 | data transfer | | data byte 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 8 | data transfer | | data byte 2 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

96 kHz IEC 958 audio DAC

UDA1351TS

8.6.7 OVERVIEW OF L3 INTERFACE REGISTERS

Table 9 UDA1351TS register map

| ADDR | FUNCTION | BIT | | | | | | | | | | | | | | | |
|--------------------------|---------------------------------|-----|-----|-----|-----|-----|------------------|------------------|----------|------|------------------|------------------|------------------|------------------|------------------|---------|---------|
| | | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| Writable settings | | | | | | | | | | | | | | | | | |
| 00H | system parameters | | | PON | | | | | | | | | | | | | |
| | default | | | 1 | | | 0 ⁽¹⁾ | 0 ⁽¹⁾ | | | 1 ⁽²⁾ | | 0 ⁽¹⁾ | 0 ⁽¹⁾ | | | |
| 10H | sound features | | | M1 | M0 | BB3 | BB2 | BB1 | BB0 | | | | TR1 | TR0 | DE1 | DE0 | MT |
| | default | | | 0 | 0 | 0 | 0 | 0 | 0 | | | | 0 | 0 | 0 | 0 | 1 |
| 11H | volume control DAC | | | | | | | | | | | VC5 | VC4 | VC3 | VC2 | VC1 | VC0 |
| | default | | | | | | | | | | | 0 | 0 | 0 | 0 | 0 | 0 |
| 40H | multiplex parameters | | | | | | | | | | | | | | | Auto MT | RST PLL |
| | default | | | | | | | | | | | 0 ⁽¹⁾ | 0 ⁽¹⁾ | 0 ⁽¹⁾ | 0 ⁽¹⁾ | 1 | 0 |
| 7FH | restore L3 defaults | | | | | | | | | | | | | | | | |
| Readable settings | | | | | | | | | | | | | | | | | |
| 18H | interpolator parameters | | | | | | | | | | | | | | | | MT stat |
| 38H | SPDIF input and lock parameters | | | | | | PLL lock | | SPD lock | ASF1 | ASF0 | PCM stat | | PRE | | ACC1 | ACC0 |

Notes

1. When writing new settings via the L3 interface, these bits should always remain at logic 0 (default value) to warrant correct operation.
2. When writing new settings via the L3 interface, these bits should always remain at logic 1 (default value) to warrant correct operation.

96 kHz IEC 958 audio DAC

UDA1351TS

8.6.8 WRITABLE REGISTERS

8.6.8.1 Restoring L3 defaults

By writing to the 7FH register, all L3 control values are restored to their default values. Only the L3 interface is affected: the system will not be reset. Consequently, readable registers that are not reset can be affected.

8.6.8.2 Power-on

A 1-bit value to switch the DAC on and off.

Table 10 Power-on setting

| PON | FUNCTION |
|-----|----------------------------|
| 0 | Power-down |
| 1 | power-on (default setting) |

8.6.8.3 Filter mode selection

A 2-bit value to program the mode for the sound processing filters of bass boost and treble.

Table 11 Filter mode settings

| M1 | M0 | FUNCTION |
|----|----|------------------------|
| 0 | 0 | flat (default setting) |
| 0 | 1 | minimum |
| 1 | 0 | |
| 1 | 1 | maximum |

8.6.8.4 Treble

A 2-bit value to program the treble setting, in combination with the filter mode settings. At $f_s = 44.1$ kHz, the -3 dB point for minimum setting is 3.0 kHz and the -3 dB point for maximum setting is 1.5 kHz. The default value is '00'.

Table 12 Treble settings

| TR1 | TR0 | LEVEL (dB) | | |
|-----|-----|------------|------|------|
| | | FLAT | MIN. | MAX. |
| 0 | 0 | 0 | 0 | 0 |
| 0 | 1 | 0 | 2 | 2 |
| 1 | 0 | 0 | 4 | 4 |
| 1 | 1 | 0 | 6 | 6 |

8.6.8.5 Bass boost

A 4-bit value to program the bass boost setting, in combination with the filter mode settings. At $f_s = 44.1$ kHz, the -3 dB point for minimum setting is 250 Hz and the -3 dB point for maximum setting is 300 Hz. The default value is '0000'.

Table 13 Bass boost settings

| BB3 | BB2 | BB1 | BB0 | LEVEL (dB) | | |
|-----|-----|-----|-----|------------|------|------|
| | | | | FLAT | MIN. | MAX. |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 1 | 0 | 2 | 2 |
| 0 | 0 | 1 | 0 | 0 | 4 | 4 |
| 0 | 0 | 1 | 1 | 0 | 6 | 6 |
| 0 | 1 | 0 | 0 | 0 | 8 | 8 |
| 0 | 1 | 0 | 1 | 0 | 10 | 10 |
| 0 | 1 | 1 | 0 | 0 | 12 | 12 |
| 0 | 1 | 1 | 1 | 0 | 14 | 14 |
| 1 | 0 | 0 | 0 | 0 | 16 | 16 |
| 1 | 0 | 0 | 1 | 0 | 18 | 18 |
| 1 | 0 | 1 | 0 | 0 | 18 | 20 |
| 1 | 0 | 1 | 1 | 0 | 18 | 22 |
| 1 | 1 | 0 | 0 | 0 | 18 | 24 |
| 1 | 1 | 0 | 1 | 0 | 18 | 24 |
| 1 | 1 | 1 | 0 | 0 | 18 | 24 |
| 1 | 1 | 1 | 1 | 0 | 18 | 24 |

8.6.8.6 De-emphasis

A 2-bit value to enable the digital de-emphasis filter.

Table 14 De-emphasis selection

| DE1 | DE0 | FUNCTION |
|-----|-----|-------------------------|
| 0 | 0 | other (default setting) |
| 0 | 1 | $f_s = 32.0$ kHz |
| 1 | 0 | $f_s = 44.1$ kHz |
| 1 | 1 | $f_s = 48.0$ kHz |

96 kHz IEC 958 audio DAC

UDA1351TS

8.6.8.7 *Soft mute*

A 1-bit value to enable the digital mute.

Table 15 Soft mute selection

| MT | FUNCTION |
|----|--------------------------|
| 0 | no muting |
| 1 | muting (default setting) |

8.6.8.8 *Volume control*

A 6-bit value to program the left and right channel volume attenuation. The range is from 0 to $-\infty$ dB in steps of 1 dB.

Table 16 Volume settings

| VC5 | VC4 | VC3 | VC2 | VC1 | VC0 | VOLUME (dB) |
|-----|-----|-----|-----|-----|-----|-------------|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 0 | 0 | 1 | 0 |
| 0 | 0 | 0 | 0 | 1 | 0 | -1 |
| 0 | 0 | 0 | 0 | 1 | 1 | -2 |
| : | : | : | : | : | : | : |
| 1 | 1 | 0 | 0 | 1 | 1 | -51 |
| 1 | 1 | 0 | 1 | 0 | 0 | |
| 1 | 1 | 0 | 1 | 0 | 1 | -52 |
| 1 | 1 | 0 | 1 | 1 | 0 | |
| 1 | 1 | 0 | 1 | 1 | 1 | -54 |
| 1 | 1 | 1 | 0 | 0 | 0 | |
| 1 | 1 | 1 | 0 | 0 | 1 | -57 |
| 1 | 1 | 1 | 0 | 1 | 0 | |
| 1 | 1 | 1 | 0 | 1 | 1 | |
| 1 | 1 | 1 | 1 | 0 | 0 | -60 |
| 1 | 1 | 1 | 1 | 0 | 1 | |
| 1 | 1 | 1 | 1 | 1 | 0 | $-\infty$ |
| 1 | 1 | 1 | 1 | 1 | 1 | |

8.6.8.9 *Auto mute*

A 1-bit value to activate mute during out-of-lock. In normal operation, the output is automatically hard muted when an out-of-lock situation is detected. Setting this bit to logic 0 will disable that function.

Table 17 Auto mute setting

| Auto MT | FUNCTION |
|---------|--|
| 0 | do not mute output during out-of-lock |
| 1 | mute output during out-of-lock (default setting) |

8.6.8.10 *PLL reset*

A 1-bit value to reset the PLL. This is the bit which is set in the initialization string. When this bit is asserted, the PLL will be reset and the output clock of the PLL will be forced to its lowest value, which is in the area of a few MHz.

Table 18 PLL reset

| RST PLL | FUNCTION |
|---------|----------------------------|
| 0 | normal operation (default) |
| 1 | PLL is reset |

8.6.9 READABLE REGISTERS

8.6.9.1 *Mute status*

A 1-bit value indicating whether the interpolator is muting or not muting.

Table 19 Interpolator mute status

| MT stat | FUNCTION |
|---------|-----------|
| 0 | no muting |
| 1 | muting |

8.6.9.2 *PLL lock detection*

A 1-bit value indicating that the clock regeneration is locked.

Table 20 PLL lock indication

| PLL lock | FUNCTION |
|----------|-------------|
| 0 | out-of-lock |
| 1 | locked |

96 kHz IEC 958 audio DAC

UDA1351TS

8.6.9.3 SPDIF lock detection

A 1-bit value indicating the IEC 958 decoder is locked and is decoding correct data.

Table 21 SPDIF lock detection

| SPD lock | FUNCTION |
|----------|--|
| 0 | not locked or non-PCM data detected |
| 1 | locked and PCM data detected |

8.6.9.4 Audio sample frequency detection

A 2-bit value indicating the audio sample frequency of the IEC 958 input signal.

Table 22 Audio sample frequency detection

| ASF1 | ASF0 | FUNCTION |
|------|------|-----------|
| 0 | 0 | 44.1 kHz |
| 0 | 1 | undefined |
| 1 | 0 | 48.0 kHz |
| 1 | 1 | 32.0 kHz |

8.6.9.5 PCM detection

A 1-bit value which indicates whether the IEC 958 input contains PCM audio data or other binary data.

Table 23 Two channel PCM input detection

| PCM stat | FUNCTION |
|----------|------------------------------------|
| 0 | input with two channel PCM data |
| 1 | input without two channel PCM data |

8.6.9.6 Pre-emphasis detection

A 1-bit value that indicates whether the pre-emphasis bit was set on the IEC 958 input signal or not set.

Table 24 Pre-emphasis detection

| PRE | FUNCTION |
|-----|-----------------|
| 0 | no pre-emphasis |
| 1 | pre-emphasis |

8.6.9.7 Clock accuracy detection

A 2-bit value indicating whether the timing accuracy of the IEC 958 input signal conforms to the IEC 958 specification.

Table 25 Input signal accuracy detection

| ACC1 | ACC0 | FUNCTION |
|------|------|-----------|
| 0 | 0 | level II |
| 0 | 1 | level I |
| 1 | 0 | level III |
| 1 | 1 | undefined |

96 kHz IEC 958 audio DAC

UDA1351TS

9 LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

| SYMBOL | PARAMETER | CONDITIONS | MIN. | MAX. | UNIT |
|----------------|--------------------------------|--|-------|-------|------|
| V_{DD} | supply voltage | note 1 | 2.7 | 5.0 | V |
| T_{xtal} | crystal temperature | | -25 | +150 | °C |
| T_{stg} | storage temperature | | -65 | +125 | °C |
| T_{amb} | ambient temperature | | -40 | +85 | °C |
| V_{es} | electrostatic handling voltage | Human Body Model (HBM); note 2 | -2000 | +2000 | V |
| | | Machine Model (MM); note 3 | -200 | +200 | V |
| $I_{lu(prot)}$ | latch-up protection current | $T_{amb} = 125\text{ °C}; V_{DD} = 3.6\text{ V}$ | - | 200 | mA |
| $I_{sc(DAC)}$ | short-circuit current of DAC | $T_{amb} = 0\text{ °C}; V_{DD} = 3\text{ V};$ note 4 | | | |
| | | output short circuited to $V_{SSA(DAC)}$ | - | 482 | mA |
| | | output short circuited to $V_{DDA(DAC)}$ | - | 346 | mA |

Notes

1. All V_{DD} and V_{SS} connections must be made to the same power supply.
2. JEDEC class 2 compliant.
3. JEDEC class B compliant, except pin $V_{SSA(PLL)}$, which can withstand ESD pulses of -130 to +130 V.
4. DAC operation after short circuiting cannot be warranted.

10 THERMAL CHARACTERISTICS

| SYMBOL | PARAMETER | CONDITIONS | VALUE | UNIT |
|---------------|---|-------------|-------|------|
| $R_{th(j-a)}$ | thermal resistance from junction to ambient | in free air | 85 | K/W |

96 kHz IEC 958 audio DAC

UDA1351TS

11 CHARACTERISTICS

$V_{DD} = V_{DDA} = 3.0$ V; IEC 958 input with $f_s = 48.0$ kHz; $T_{amb} = 25$ °C; $R_L = 5$ k Ω ; all voltages measured with respect to ground; unless otherwise specified.

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|--|---------------------------------|------------------------------------|---------------|---------------|----------------|------------|
| Supplies; note 1 | | | | | | |
| V_{DDA} | analog supply voltage | | 2.7 | 3.0 | 3.6 | V |
| $V_{DDA(DAC)}$ | analog supply voltage for DAC | | 2.7 | 3.0 | 3.6 | V |
| $V_{DDA(PLL)}$ | analog supply voltage for PLL | | 2.7 | 3.0 | 3.6 | V |
| V_{DDD} | digital supply voltage | | 2.7 | 3.0 | 3.6 | V |
| $V_{DDD(C)}$ | digital supply voltage for core | | 2.7 | 3.0 | 3.6 | V |
| $I_{DDA(DAC)}$ | analog supply current of DAC | power-on | – | 8.0 | – | mA |
| | | Power-down | – | 750 | – | μ A |
| $I_{DDA(PLL)}$ | analog supply current of PLL | at 48 kHz | – | 0.7 | – | mA |
| | | at 96 kHz | – | 1.0 | – | mA |
| $I_{DDD(C)}$ | digital supply current of core | at 48 kHz | – | 16.0 | – | mA |
| | | at 96 kHz | – | 24.5 | – | mA |
| I_{DDD} | digital supply current | at 48 kHz | – | 2.0 | – | mA |
| | | at 96 kHz | – | 3.0 | – | mA |
| P | power consumption at 48 kHz | DAC in playback mode | – | 80 | – | mW |
| | | DAC in Power-down mode | – | 58 | – | mW |
| | power consumption at 96 kHz | DAC in playback mode | – | 109 | – | mW |
| | | DAC in Power-down mode | – | 87 | – | mW |
| Digital input pins | | | | | | |
| V_{IH} | HIGH-level input voltage | | $0.8V_{DD}$ | – | $V_{DD} + 0.5$ | V |
| V_{IL} | LOW-level input voltage | | –0.5 | – | $+0.2V_{DD}$ | V |
| $V_{hys(RESET)}$ | hysteresis voltage on pin RESET | | – | 0.8 | – | V |
| $ I_{LI} $ | input leakage current | | – | – | 10 | μ A |
| C_i | input capacitance | | – | – | 10 | pF |
| $R_{pu(int)}$ | internal pull-up resistance | | 16 | 33 | 78 | k Ω |
| $R_{pd(int)}$ | internal pull-down resistance | | 16 | 33 | 78 | k Ω |
| Digital output pins | | | | | | |
| V_{OH} | HIGH-level output voltage | $I_{OH} = -2$ mA | $0.85V_{DD}$ | – | – | V |
| V_{OL} | LOW-level output voltage | $I_{OL} = 2$ mA | – | – | 0.4 | V |
| $I_{L(max)}$ | maximum load current | | – | 3 | – | mA |
| Digital-to-analog converter; note 2 | | | | | | |
| V_{ref} | reference voltage | measured with respect to V_{SSA} | $0.45V_{DDA}$ | $0.50V_{DDA}$ | $0.55V_{DDA}$ | V |
| $V_{o(rms)}$ | output voltage (RMS value) | | – | 900 | – | mV |

96 kHz IEC 958 audio DAC

UDA1351TS

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|----------------------|--|---|------|------|------|------------|
| (THD + N)/S | total harmonic distortion-plus-noise to signal ratio | f _i = 1.0 kHz tone at 48 kHz | – | –90 | –85 | dB |
| | | at 0 dB | – | –60 | –55 | dB |
| | | at –40 dB; A-weighted | – | –60 | –55 | dB |
| | | f _i = 1.0 kHz tone at 96 kHz | – | –85 | –80 | dB |
| | | at 0 dB | – | –57 | –52 | dB |
| | | at –40 dB; A-weighted | – | –57 | –52 | dB |
| S/N | signal-to-noise ratio at 48 kHz | f _i = 1.0 kHz tone; code = 0; A-weighted | 95 | 100 | – | dB |
| | signal-to-noise ratio at 96 kHz | f _i = 1.0 kHz tone; code = 0; A-weighted | 95 | 100 | – | dB |
| α_{cs} | channel separation | f _i = 1.0 kHz tone | – | 96 | – | dB |
| ΔV_o | unbalance of output voltages | f _i = 1.0 kHz tone | – | 0.1 | 0.4 | dB |
| IEC 958 input | | | | | | |
| V _{i(p-p)} | AC input voltage (peak-to-peak value) | | 0.2 | 0.5 | 3.3 | V |
| R _i | input resistance | | – | 6 | – | k Ω |
| V _{hys} | hysteresis voltage | | – | 40 | – | mV |

Notes

1. All supply pins V_{DD} and V_{SS} must be connected to the same external power supply unit.
2. When the DAC must drive a higher capacitive load (above 50 pF), a series resistor of 100 Ω must be used to prevent oscillations in the output stage of the operational amplifier.

96 kHz IEC 958 audio DAC

UDA1351TS

12 TIMING CHARACTERISTICS

$V_{DD} = V_{DDA} = 2.7$ to 3.6 V; $T_{amb} = -40$ to $+85$ °C; $R_L = 5$ k Ω ; all voltages measured with respect to ground; unless otherwise specified.

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | UNIT |
|---|--|------------------|------|------|---------|
| Device reset | | | | | |
| t_{rst} | reset active time | | – | 250 | μ s |
| PLL lock time | | | | | |
| t_{lock} | time to lock | $f_s = 32.0$ kHz | – | 85.0 | ms |
| | | $f_s = 44.1$ kHz | – | 63.0 | ms |
| | | $f_s = 48.0$ kHz | – | 60.0 | ms |
| | | $f_s = 48.0$ kHz | – | 40.0 | ms |
| Microcontroller L3 interface timing (see Figs 8 and 9) | | | | | |
| $T_{cy(CLK)(L3)}$ | L3CLOCK cycle time | | 500 | – | ns |
| $t_{CLK(L3)H}$ | L3CLOCK HIGH time | | 250 | – | ns |
| $t_{CLK(L3)L}$ | L3CLOCK LOW time | | 250 | – | ns |
| $t_{su(L3)A}$ | L3MODE set-up time for address mode | | 190 | – | ns |
| $t_{h(L3)A}$ | L3MODE hold time for address mode | | 190 | – | ns |
| $t_{su(L3)D}$ | L3MODE set-up time for data transfer mode | | 190 | – | ns |
| $t_{h(L3)D}$ | L3MODE hold time for data transfer mode | | 190 | – | ns |
| $t_{(stp)(L3)}$ | L3MODE stop time in data transfer mode | | 190 | – | ns |
| $t_{su(L3)DA}$ | L3DATA set-up time in address and data transfer mode | | 190 | – | ns |
| $t_{h(L3)DA}$ | L3DATA hold time in address and data transfer mode | | 30 | – | ns |
| $t_{su(L3)R}$ | L3DATA set-up time in data transfer mode | read mode | 50 | – | – |
| $t_{h(L3)R}$ | L3DATA hold time in data transfer mode | read mode | 360 | – | – |

96 kHz IEC 958 audio DAC

UDA1351TS

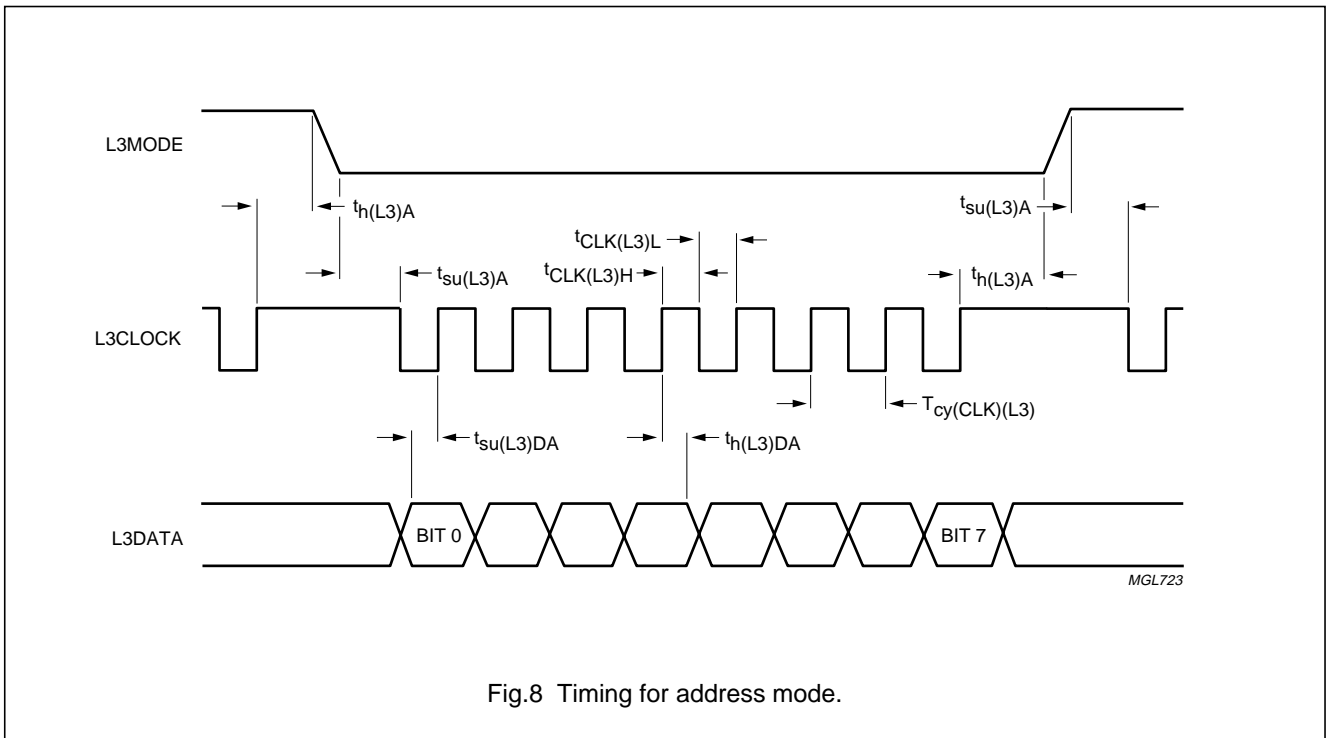


Fig.8 Timing for address mode.

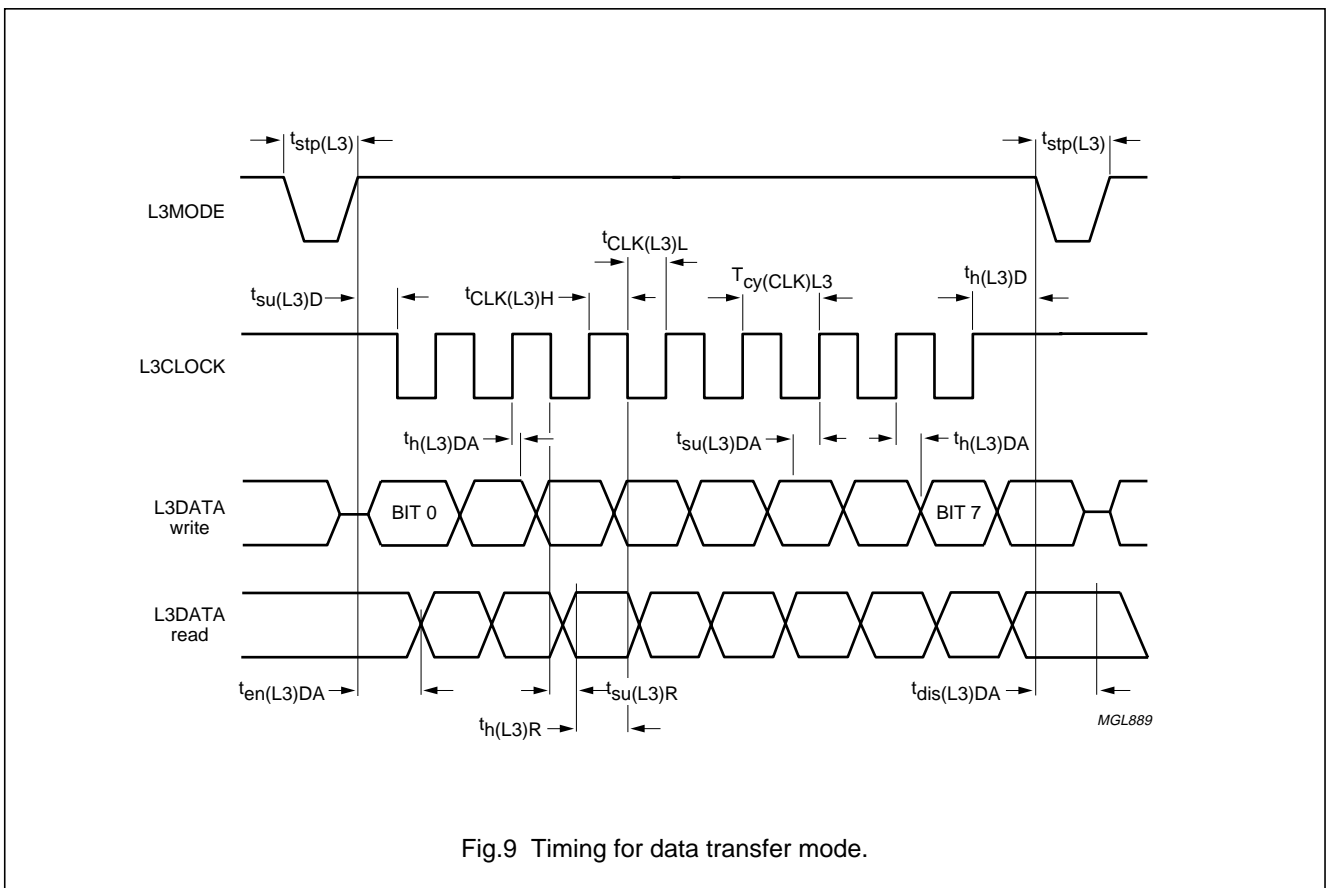


Fig.9 Timing for data transfer mode.

96 kHz IEC 958 audio DAC

UDA1351TS

13 APPLICATION INFORMATION

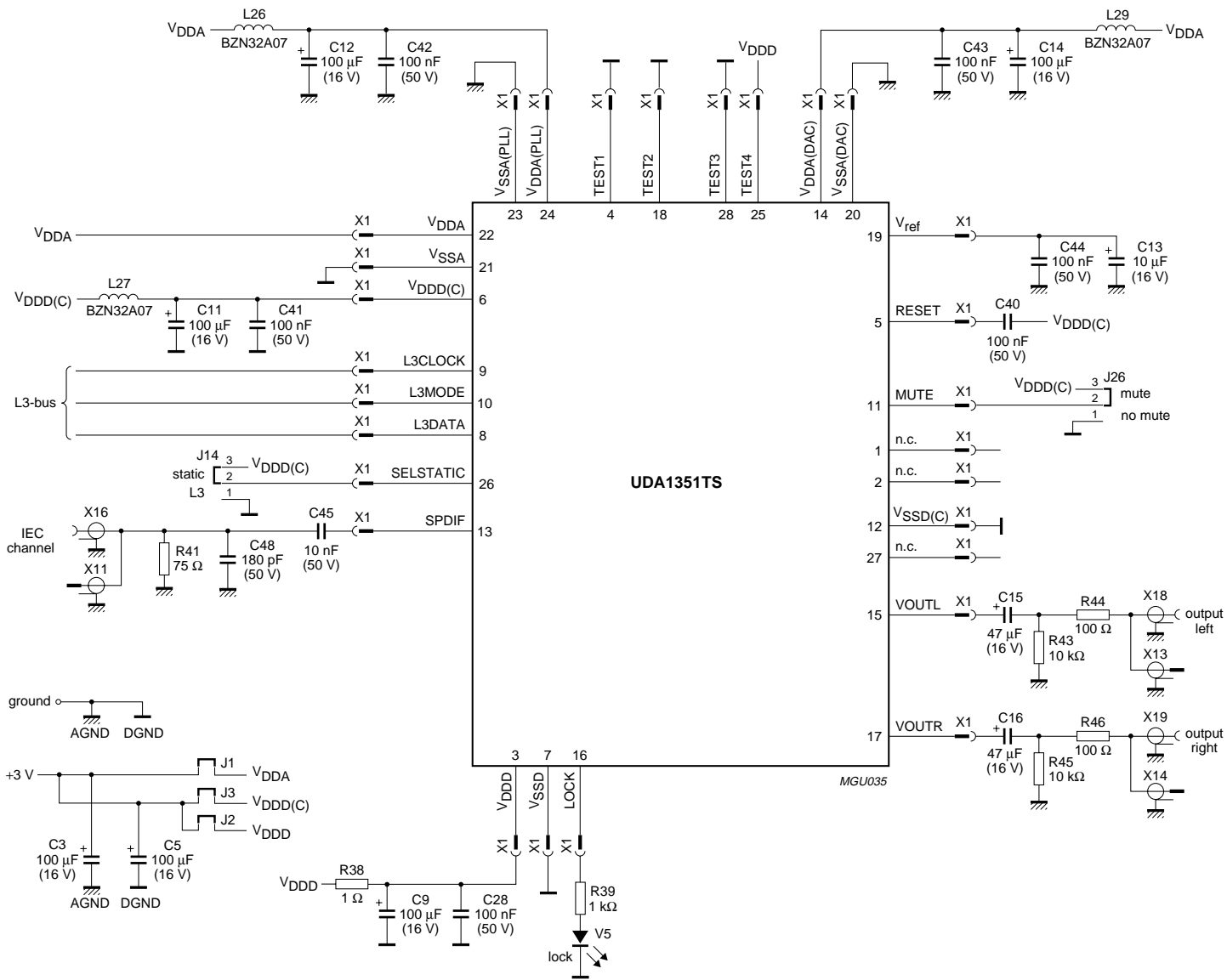


Fig.10 Test and application diagram.

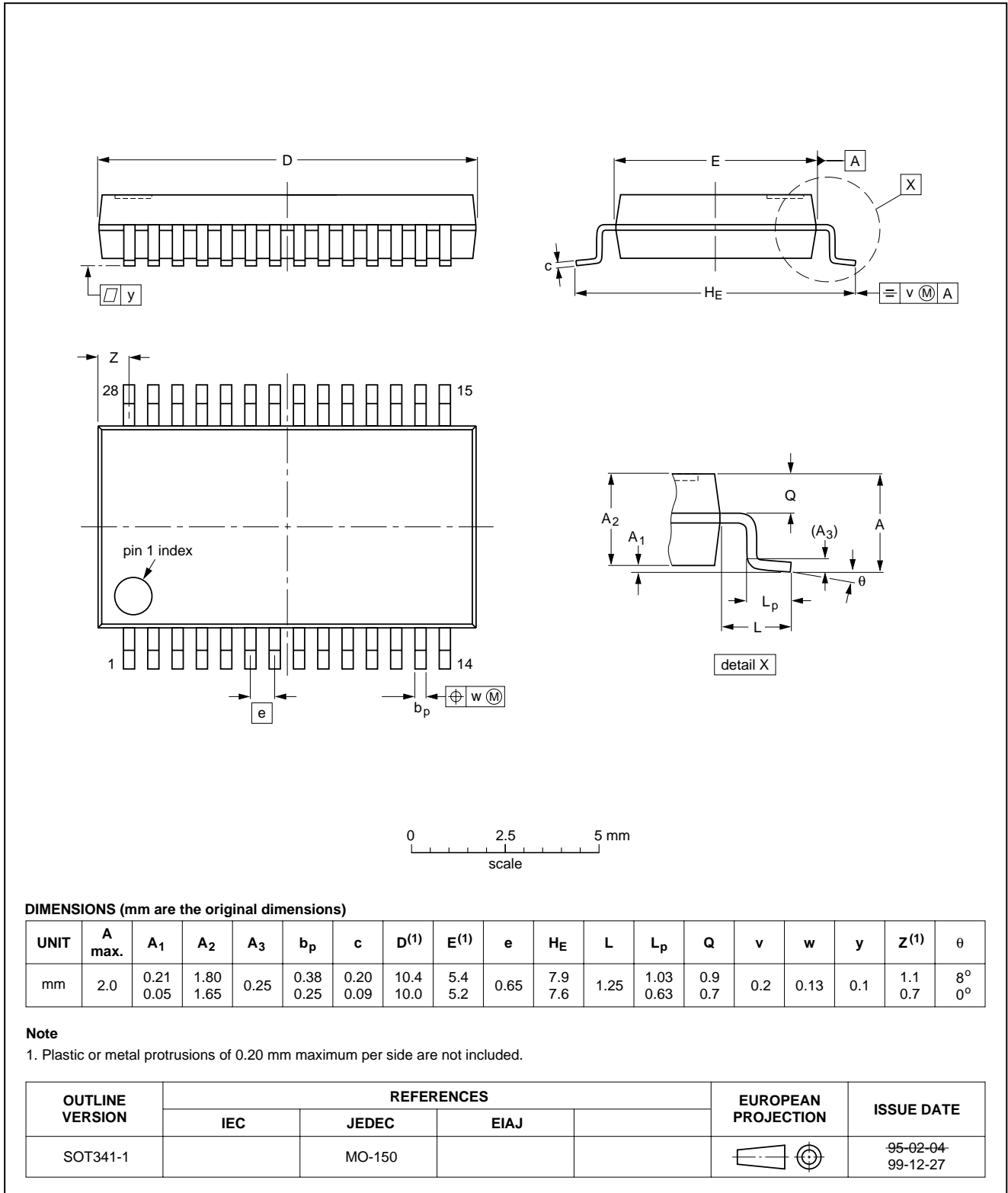
96 kHz IEC 958 audio DAC

UDA1351TS

14 PACKAGE OUTLINE

SSOP28: plastic shrink small outline package; 28 leads; body width 5.3 mm

SOT341-1



96 kHz IEC 958 audio DAC

UDA1351TS

15 SOLDERING**15.1 Introduction to soldering surface mount packages**

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *“Data Handbook IC26; Integrated Circuit Packages”* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering is not always suitable for surface mount ICs, or for printed-circuit boards with high population densities. In these situations reflow soldering is often used.

15.2 Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, infrared/convection heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferably be kept below 230 °C.

15.3 Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
 - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
 - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

The footprint must incorporate solder thieves at the downstream end.
- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C. A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

15.4 Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

96 kHz IEC 958 audio DAC

UDA1351TS

15.5 Suitability of surface mount IC packages for wave and reflow soldering methods

| PACKAGE | SOLDERING METHOD | |
|--|-----------------------------------|-----------------------|
| | WAVE | REFLOW ⁽¹⁾ |
| BGA, LFBGA, SQFP, TFBGA | not suitable | suitable |
| HBCC, HLQFP, HSQFP, HSOP, HTQFP, HTSSOP, SMS | not suitable ⁽²⁾ | suitable |
| PLCC ⁽³⁾ , SO, SOJ | suitable | suitable |
| LQFP, QFP, TQFP | not recommended ⁽³⁾⁽⁴⁾ | suitable |
| SSOP, TSSOP, VSO | not recommended ⁽⁵⁾ | suitable |

Notes

1. All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *“Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods”*.
2. These packages are not suitable for wave soldering as a solder joint between the printed-circuit board and heatsink (at bottom version) can not be achieved, and as solder may stick to the heatsink (on top version).
3. If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
4. Wave soldering is only suitable for LQFP, TQFP and QFP packages with a pitch (e) equal to or larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
5. Wave soldering is only suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

96 kHz IEC 958 audio DAC

UDA1351TS

16 DATA SHEET STATUS

| DATA SHEET STATUS | PRODUCT STATUS | DEFINITIONS ⁽¹⁾ |
|---------------------------|----------------|--|
| Objective specification | Development | This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice. |
| Preliminary specification | Qualification | This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product. |
| Product specification | Production | This data sheet contains final specifications. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product. |

Note

1. Please consult the most recently issued data sheet before initiating or completing a design.

17 DEFINITIONS

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

Application information — Applications that are described herein for any of these products are for illustrative purposes only. Philips Semiconductors make no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

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UDA1351TS

NOTES

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SCA 71

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Printed in The Netherlands

753503/02/pp32

Date of release: 2001 Feb 05

Document order number: 9397 750 07921

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